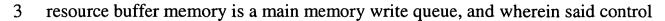**We Claim:**

1   1.   In a graphics system including a main processor and a graphics

2   processing system for generating graphics images on a display in cooperation with

3   said main processor, and a memory, said system including a plurality of resources

4   seeking access to said memory, a memory controller comprising:

5   a plurality of buffer memories, each of said buffer memories being

6   operatively coupled to one of said plurality of resources seeking access to said

7   memory for storing information indicative of a request for memory access;

8   a multiple resource buffer memory coupled to said first plurality of buffer

9   memories for storing requests for memory access requests from each of said

10   plurality of resources; and

11   a control circuit for controlling the transfer of information from said first

12   plurality of buffer memories to said multiple resource buffer memory, wherein said

13   control circuit is operable to control the transfer of information from said first

14   plurality of buffer memories to said multiple resource buffer memory to reduce the

15   frequency of switching from main memory write operations to main memory read

16   operations.

1   2.   A memory controller according to claim 1, wherein said plurality of

2   buffer memories are main memory write queues.

1   3.   A memory controller according to claim 1, wherein said multiple

2   resource buffer memory is a main memory write queue.

1   4.   A memory controller according to claim 1, wherein said plurality of

2   buffer memories are main memory write queues, and wherein said multiple

3   resource buffer memory is a main memory write queue, and wherein said control

4   circuit is operable to control the rate at which write requests are coupled to the

5   multiple resource buffer memory from the plurality of buffer memories.

1   5.   A memory controller according to claim 1, wherein said plurality of

2   buffer memories are main memory write queues and further including a plurality of

3   main memory read queues, each read queue being operatively coupled to a

4   resource seeking to read information from said main memory.

1   6.   A memory controller according to claim 1, wherein said control

2   circuit includes arbitration circuitry for granting requests for access to main

3   memory.

1   7.   A memory controller according to claim 6, wherein said arbitration

2   circuitry is operable to control the frequency with which the requesting resources

3   are enabled to participate in the arbitration for main memory access.

1   8.   A memory controller according to claim 1, further including a

2   memory access control register associated with one of said resources, wherein said

3   arbitration control circuit includes arbitration circuitry responsive to the contents of

4   said memory access control register for determining the frequency that said

5   resource is permitted to participate in memory access arbitration.

1   9.   A memory controller according to claim 1, further including a set of

2   control registers, said control registers being programmable by said main

3   processor.

1   10.   A memory controller according to claim 9, wherein said control

2   circuitry is operable to arbitrate between said resources for granting requests for

3   memory access, wherein said control registers include a plurality of memory

4   bandwidth control registers which are accessed by said control circuitry in

5   determining which resource will be granted memory access.

1   11.   A memory controller according to claim 10, wherein each of said

2   memory bandwidth control registers is respectively associated with a resource

3   seeking main memory access.

1   12.   A memory controller according to claim 9, wherein said control

2   registers include at least one register associated with a memory access requesting

3   resource for storing data for said requesting resource indicative of at least one of

4   memory usage and memory bandwidth for that resource.

1   13.   A memory controller according to claim 9, wherein said control

2   registers include at least one register associated with a memory access requesting

3   resource for storing data for said requesting resource indicative of wasted memory

4   cycles due to granting memory access to that resource.

1   14.   A memory controller according to claim 1, wherein said plurality of

2   buffer memories and said multiple resource buffer memory are write request

3   queues, and wherein a resource that is writing to main memory generates a flush

4   signal for initiating the flushing of that resource's write request queue.

1   15.   A memory controller according to claim 14, further including a flush

2   acknowledge handshake signal generating circuit that generates a flush

3   acknowledge handshake signal to thereby indicate to competing resources that data

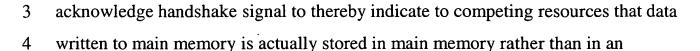4   written to main memory is actually stored in main memory rather than in an

5   associated resource's buffer.

1   16.   In an information processing system including a main processor, a

2   memory, and at least a first and a second resource competing with said main

3   processor for access to said memory, a memory controller comprising:

4   a main processor related interface including a main processor read request

5   queue and a main processor write request queue;

6   a first resource related interface including at least one of a first resource read

7   request queue and a first resource write request queue;

8   a second resource related interface including at least one of a second

9   resource read request queue and a second resource write request queue;

10   a multiple resource write queue for receiving requests for writing to said

11   main memory; and

12   a memory access control circuit for granting access to said main memory,

13   said memory access control circuit being coupled to receive read requests from

14   each of said read queues and for receiving write requests from said multiple

15   resource write queue.

1   17.   A memory controller according to claim 16, wherein said control

2   circuit is operable to control the transfer of information from said main processor

3   write queue, said first resource write queue and said second resource write queue

4   to said multiple resource write queue to thereby reduce the frequency of switching

5   from main memory write operations to main memory read operations.

1   18.   A memory controller according to claim 16, wherein said memory

2   access control circuitry is operable to arbitrate among resources competing for

3   memory access and to control the frequency with which requesting resources are

4   enabled to participate in the arbitration.

1   19.   A memory controller according to claim 16, further including a

2   memory access control register associated with one of said resources, wherein said

3   memory access control circuit includes arbitration circuitry responsive to the

4   contents of said memory access control register for determining the frequency that

5   said resource is permitted to participate in memory access arbitration.

1   20.   A memory controller according to claim 16, further including a set of

2   control registers, said control registers being programmable by said main

3   processor.

1   21.   A memory controller according to claim 20, wherein said memory

2   access control circuit is operable to arbitrate between said resources for granting

3   requests for memory access, wherein said control registers include a plurality of

4   memory bandwidth control registers which are accessed by said memory access

5   control circuit in determining which resource will be granted memory access.

1   22.   A memory controller according to claim 21, wherein each of said

2   memory bandwidth control registers is respectively associated with a resource

3   seeking main memory access.

1   23.   A memory controller according to claim 20, wherein said control

2   registers include at least one performance related register associated with a

3   memory access requesting resource for storing data for said requesting resource

4   indicative of at least one of memory usage and memory bandwidth for that

5   resource.

1   24.   A memory controller according to claim 20, wherein said control

2   registers include at least one performance related register associated with a

3   memory access requesting resource for storing data for said requesting resource

4   indicative of wasted memory cycles due to granting memory access to that

5   resource.

1   25.   A memory controller according to claim 16, wherein a resource that is

2   writing to main memory generates a flush signal for initiating the flushing of that

3   resource's write request queue.

1   26.   A memory controller according to claim 25, further including a flush

2   acknowledge handshake signal generating circuit to generate a flush acknowledge

3   handshake signal and thereby indicate to competing resources that data written to

4   main memory is actually stored in main memory rather than in an associated

5   resource buffer.

1   27.   In an information system including a main processor, a memory, and

2   at least a first and a second resource competing with said main processor for access

3   to said memory, a method of controlling access to said main memory comprising

4   the steps of:

5   storing requests for main memory access from a first resource in a first

6   resource request queue;

7   storing requests for main memory access from a second resource in a second

8   resource request queue;

9   delaying forwarding requests for memory access to a memory access control

10 circuit to reduce the frequency of switching between memory read states and

11 memory write states; and

12 granting requests for memory access by said memory access control circuit.

1   28.   A method according to claim 27, wherein said step of delaying

2   includes the step of storing requests in a multiple resource write queue.

1   29.   A method according to claim 27, further including the step of storing

2   requests for main memory access by said main processor in a main processor

3   request queue.

1   30.   A method according to claim 27, wherein said step of granting

2   requests for memory access includes the step of arbitrating among competing

3   resources and further including the step of controlling the frequency with which

4   requesting resources are enabled to participate in memory access arbitration.

1   31.   A method according to claim 30, wherein the step of controlling the

2   frequency includes the step of accessing contents of a memory access control

3   register associated with a resource for determining the frequency that said resource

4   is permitted to participate in memory access arbitration.

1   32.   A method according to claim 27 further including the step of

2   controlling memory access by programming at least one of a set of control registers

3   in said memory controller by said main processor.

1   33.   A method according to claim 27, wherein said step of granting

2   memory access includes the step of arbitrating between said resources for granting

3   requests for memory access, and further including the step of accessing a plurality

4   of memory bandwidth control registers and determining which resource will be

5   granted memory access in part based upon the contents of said memory bandwidth

6   control registers.

1   34.   A method according to claim 33, further including the step of

2   associating each of said memory bandwidth control registers with a resource

3   seeking main memory access.

1   35.   A method according to claim 27, further including the step of storing

2   data relating to a requesting resource indicative of at least one of memory usage

3   and memory bandwidth for that resource.

1   36.   A method according to claim 27, further including the step of storing

2   data for a requesting resource indicative of wasted memory cycles due to granting

3   memory access to that resource.

1   37.   A method according to claim 27, further including the step of writing

2   data by a resource to main memory and generating a buffer flush signal for

3   initiating the flushing of that resource's write request queue.

1   38.   A method according to claim 37, further including the step of

2   generating a flush acknowledge handshake signal to competing resources that data

3   written to main memory is actually stored in main memory rather than in an
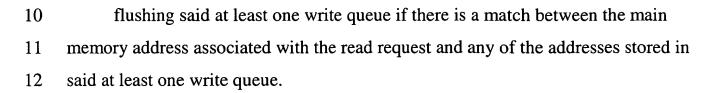
4   associated resource's buffer.

1   39.   A method according to claim 27, wherein the step of granting requests
2   includes the step of fulfilling requests for memory access in the order requested.

1   40.   In an information system including a main processor, a memory, and
2   at least a first and a second resource competing with said main processor for access
3   to said memory, a method of controlling access to said main memory comprising
4   the steps of:

5   storing requests for writing to main memory from a first resource in a first
6   resource write request queue;

7   writing to main memory by said first resource;

8   generating a write queue flush signal by said first resource to initiate
9   copying information in said first resource write request queue to main memory;
10   and

11   flushing said first resource write request queue.

1   41.   A method according to claim 40, further including the step of
2   generating a flush acknowledge handshake signal to competing resources that data
3   written to main memory is actually stored in main memory rather than in said first
4   resource write queue.

5   42.   A method according to claim 40, further including the steps of

6   storing requests for reading from main memory from a second resource in a
7   second resource read request queue;

8   comparing the main memory address associated with the read request with
9   the addresses stored in at least one write queue; and

10   flushing said at least one write queue if there is a match between the main

11   memory address associated with the read request and any of the addresses stored in

12   said at least one write queue.

1   43.   A method according to claim 40, further including the steps of storing

2   requests for writing to main memory from a second resource in a second resource

3   write request queue;

4   delaying forwarding requests for memory access to a memory access control

5   circuit to reduce the frequency of switching between memory read states and

6   memory write states; and

7   granting requests for memory access by said memory access control circuit.

1   44.   A method according to claim 43, wherein said step of delaying

2   includes the step of storing requests in a multiple resource write queue.

1   45.   A method according to claim 40, further including the step of storing

2   requests for main memory access by said main processor in a main processor

3   request queue.

1   46.   A method according to claim 40, further including the steps of

2   arbitrating requests for memory access among competing resources and

3   controlling the frequency with which requesting resources are enabled to

4   participate in memory access arbitration.

1   47.   A method according to claim 46, wherein the step of controlling the

2   frequency includes the step of accessing the contents of a memory access control

3   register associated with a resource for determining the frequency that said resource

4   is permitted to participate in memory access arbitration.

1   48.   A method according to claim 40, further including the step of

2   controlling memory access by programming at least one of a set of control registers

3   in said memory controller by said main processor.

1   49.   A method according to claim 40, further including the steps of

2   arbitrating memory access requests between said resources by accessing a plurality

3   of memory bandwidth control registers and determining which resource will be

4   granted memory access in part based upon the contents of said memory bandwidth

5   control registers.

1   50.   A method according to claim 49, further including the step of

2   associating each of said memory bandwidth control registers with a resource

3   seeking main memory access.

1   51.   A method according to claim 40, further including the step of storing

2   data relating to a requesting resource indicative of at least one of memory usage

3   and memory bandwidth for that resource.

1   52.   A method according to claim 40, further including the step of storing

2   data for a requesting resource indicative of wasted memory cycles due to granting

3   memory access to that resource.

1   53.   A method according to claim 40, further including the step of

2   fulfilling requests for memory access in the order requested.

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